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Form PTO-1449J.S. Department of Commerce Patent and Trademark Office.			Docket No. D5116-0000	/		Serial No. 09/675,427		
	INFORMATION DISCLOSURE STATEMENT		Applicant Saxena et al.	MAY 2 5 2001				
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H.D.	AA	5,767,542	6/16/98	Nakamura	57	296		
H.D.	AB	5,773,315	6/30/98	Jarvis	438	14		
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H.D.	А	International Search Report date	d 09 APR 2001		 			
H.D.	В	Khare et al., "Extraction of IEEE, May 1991, pages 4		acteristics for Yield Estimation Us	ing The Dou	ible Bridge Test	Structur	e",
H.D.	С	Yun et al., "Evaluating the Using Neural Networks, I		bility of GaAs/AIGaAs Multiple Q 7, pages 105-112	uantum We	ll Avalanche Ph	otodiode	S
H.D.	D	Hansen et al., "Effectiven Measurements", IEEE, Ja		stimation and Reliability-Prediction 142-148	n Based on	Wafer Test-Chip	- 	
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H. D.	A	3,751,647	8/1/13	Maeder et al.	235	151.11		
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H.D.	D	Khare et al., "Yield Oriented C Vol. 8, No. 02, May 1995 (02.		ided Defect Diagnosis", IEEE Tra ages 195-206	ns. on Semi	onductor Mai	ıufacturın	g,
H.D.	E	International Search Report da	ited 08 JUN	2001				

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H.D.	В	Nurani et al., "In-Line Yield F Transactions on Semiconducto				on Information	", IEEE	
								
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STA	STATEMENT BY APPLICANT		First Named Inventor	Sharad Saxena Technology Center	
	(the se mean she	- 4		Art Unit	2128
(Use as many sheets as necessary)			19cessery)	Examiner Name	Morella I Rosales Hanner
Sheet	1	of	2	Attorney Docket Number	D5116-00002

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
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Examiner Signature	Henry-Mer Days	Date Considered	3/24/05
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	Complete if Known	
Application Number	09/675,427	
Filing Date	September 29, 2000	
First Named Inventor	Sharad Saxena	
Art Unit	2128	
Examiner Name	Morella i Rosales Hanner	
Attorney Docket Number	D5116-00002	

NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of Examiner Cite No.1 the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue T² Initials* number(s), publisher, city and/or country where published. PELGROM et al., "Matching Properties of MOS Transistors." IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, SC-24, pp. 1433-1440, October 1989 H.D. SIDNEY SOCLOF, "Design and Applications of Analog Integrated Circuits." Prentice Hall, New HD Jersey, 1991. STROJWAS et al., "Manufacturability of Low-Power CMOS Technology Solutions." Invited Paper, International Symposium on Low-Power Electronics and Design, Monterey (CA), August 1996 HD TUINHOUT et al., "Matching of MOS Transistors." FSA Modeling Workshop, San Jose (CA), May H.D 1999 VELGHE et al., "Compact MOS Modelling for Analogue Circuit Simulation." IEDM Techn. Digest, HD pp. 485-488, Washing (DC), 1993 ZHANG et al., "Yield and Variability Optimization of Integrated Circuits." Kluwer Academic HD Publishers, Boston, 1995 HANSON et al., "Analysis of Mixed-Signal Manufacturabiltiy with Statistical Technology CAD H.D. (TCAD), IEEE Transactions on Semiconductor Manufacturing, Vol. 9, No. 4, November 1996 RECEIVED AUG 2 7 2004 **Technology Center 2100**

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